International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 10, No. 3, Sep 2019, pp. 1347~1354
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v10.i3.1347-1354

Photovoltaic fed multilevel inverter using reverse voltage topology for standalone systems

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Article Info

Article history:

Received Nov 9, 2018
Revised Jan 28, 2019
Accepted Mar 19, 2019

Keywords:

Carrier signal
Multilevelinverter
Photovoltaic cell
Spwm technique

ABSTRACT

Multilevel Inverters are generally utilized for medium voltage and high power applications. Invented in 1975, MLIs have brought huge change in the field of Electrical and Electronics. It contains distinctive topologies. This paper proposes a photovoltaic aided multilevel inverter with Reverse Voltage topology with diminished number of switches. In comparison to other existing topologies this topology utilizes minimum number of switches and less number of carrier signals which in turns diminishes the complexity of the system as well as cost. The proposed framework contains five MOSFETs, five diodes to create eleven levels. In this topology the SPWM strategy has been utilized. This topology utilizes one sine wave and five triangular waves, which is half in comparison to the existing topologies. As sustainable power sources can be utilized for multilevel inverter, photovoltaic cell has been utilized. The MATLAB recreation for both solar powered module and Multilevel inverter has been appeared alongside the equipment approach.

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1. INTRODUCTION

The presentation of Solar Energy has gotten an exceptional change the field of Electrical sciences. As it is realized that petroleum products cause natural peril, subsequently the use of solar cell has been invited. Solar cell has been recognized most widely and often utilized. As this is sustainable and clean, nowdays it has been utilized as power hotspot for various machines like multilevel inverters, electric vehicles etc[1, 2].Today the most noteworthy productivity of PV cells are stretched to 44%. This is noted by Fraunhofer Institute of Solar Energy Systems [2].

Introduced 25 years back, multilevel inverters have reformed the field of Electrical engineering. The idea requires using large number of dynamic semiconductor changes to play out the power transformation in minimized voltage levels. There are some merits of these inverters that incorporate the minimized voltage steps to create higher power quality waveforms and minimal voltage stress on the load and henceforth deducting the electromagnetic similarity concerns [3]. One more essential element of multilevel inverter is that the power semiconductors are wired in a series manner, which allows task at high voltages. Be that as it may, the series connection is regularly made with diode clipping, which disposes of overvoltage concerns. One prominent drawback of multilevel power transformation is the necessity of certain number of switches [4]. This ought to be noticed that minimal voltage appraised switches can be utilized as a part of the multilevel inverter [5, 6]. Therefore, the active semiconductor cost isn't excessively expanded when contrasted with two level inverters. Notwithstanding, every multilevel semiconductor require gate driver circuits and builds unpredictability to the converter mechanical setup [7-9]. Another drawback can be seen in the multilevel control inverter is that the minimal voltage steps are for the most part delivered by isolated

voltage sources or a series capacitor bank. Isolated voltage sources may not be accessible often and series capacitors come into play for voltage adjusting. To some point, the voltage adjusting can be tended to by utilizing recursive (repeatative) exchanging states, which exist because of the utilization of more number of semiconductor switches. However, for a total answer for the voltage-adjusting issue, a more effective multilevel inverter topology might be required [10-12].

Reverse Voltage Topology is proposed to improve the shortcomings of the existing MLI Topologies. In comparison with the existing topologies this topology includes minimum number of switches and a certain minimum number of carrier signals in order to generate required levels. This in turns reduces the overall complexity of the system. It does not require voltage balancing networks [13]. The MATLAB simulation for this topology representation has been shown as well as the hardware approach.

2. PHOTOVOLTAIC CELL AND ITS SIMULATION

Solar cell or photovoltaic cell changes over the irradiance of light straightforwardly into power by Photovoltaic impact. This is physical and chemical phenomena. It is a classification of photovoltaic cell whose electrical attributes changes with the difference in force of light. In essential terms a solar cell produces 0.5V to 0.6V as open circuit voltage.

a. Photons hit the solar panel and semiconducting material silicon present in the Solar Cell ingests it.
b. Electrons are energized from their nuclear orbital. Once energized an electron scatter heat energy subsequently coming back to orbital or going through the cell until the point that it comes back to cathode. The streaming current through the material drops the potential and power is got.
c. A series of solar cells changes over solar energy into a huge sum DC current. This can be bolstered to an inverter and the inverter changes over the current to AC Current.

The mathematical modeling for an ideal solar cell can be written likewise,

$$[\mathrm{Iph}] - \mathrm{Ie}[\mathrm{V} = \mathrm{nV\,t}] - 1 = \mathrm{I} \quad (1)$$

The mathematical modeling for an ideal solar cell can be written likewise

$$Iph = [Isc + Ki(T - 298)] \times Ir/1000 \quad (2)$$

Module reverse current equation

$$Ir = Isc/[e^{\frac{qVo}{NsKT}} - 1] \quad (3)$$

The module saturation current Io varies with temperature and will be given by,

$$Io = Irs[\frac{T}{Tr}]^3 - e^{\frac{qEo}{nk}}\left(\frac{1}{T} - \frac{1}{Tr}\right) \quad (4)$$

Solar cell has been designed using MATLAB Simulink and the simulation model has been shown in the Figure1. The Solar Cell simulation is done for 6V and the simulation outputs for V-I and P-V characteristics are shown in Figure 2 and 3.

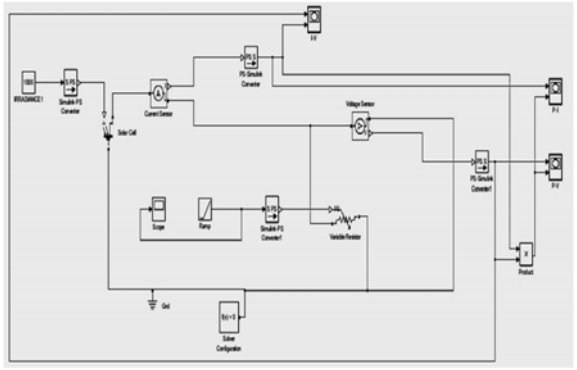

Figure 1. Solar cell using MATLAB design

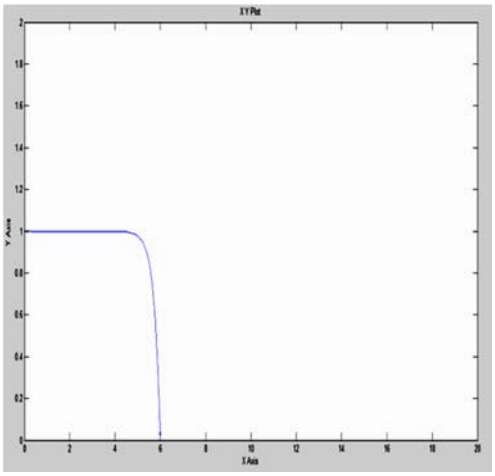

Figure 2. V-I plot for solar cell design

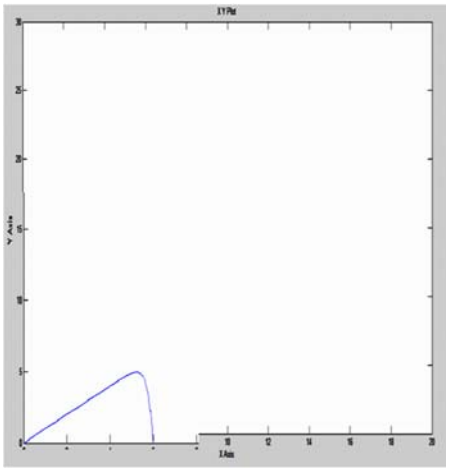

Figure 3. P-V plot for solar cell simulation design

3. MULTILEVEL INVERTER WITH REVERSE VOLTAGE TOPOLOGY

The overall block diagram of the planned system is shown in Figure.4 to minimize harmonics and torque ripple. The operation of the system is as follows: the armature current is sensed through current sensors and converted into voltage signals. These signals are then rectified and a dc component, with the value of the ceiling of the current I_{dc} is obtained as shown in Figure 4. This dc signal is compared with desired reference signal I_{ref}, and from this comparison the error signal I_{err} is obtained. This error signal is passed through a controller (PI or fuzzy) to generate the PWM pulses as shown in Fig.4 for all the switches of the three phase inverter, which are sequentially activated by the shaft position sensor.

Multilevel Inverters are the pathfinders of modern day Electrical and Electronics. Inspite of the fact that these inverters are utilized for medium voltage and high power applications, this proposed topology can likewise be connected for high power and high voltage applications [14, 15] Conventional multilevel inverters incorporate controlled semiconductor switches for creating a high recurrence waveform of both positive and negative polarities [5]. In this technique there is no compelling reason for taking into consideration all the switches to create levels at both positive and negative polarity. This technique is a hybrid multilevel topology [15], which is separated into two sections. First one is level generation unit and is responsible for positive level generation. This part requires high frequency changes for positive level generation. The switches in this part have more exchanging recurrence capacity [15] The other part works as polarity generation unit which creates the polarity of the given voltage. This part is comprised of less recurrence switches that works at line recurrence(frequency). These two sections (high frequency and low frequency) work together to produce a complete multilevel voltage waveform.

For generating a total multilevel output wave, the positive levels generated by level generating unit is fed into a full bridge inverter which comes into play to produce required polarity for the output. This reduces the usage of more semiconductor switches. The existing system contains 8 MOSFETs and 8 diodes to generate 11-levels [7]. Hence in comparison to the existing topology the proposed topology contains only 5 MOSFETs and 5 feedback diodes in order to generate 11-Levels.For SPWM techniques only five carrier signal has been used.

Switching sequence of this inverter is simpler than the conventional inverters. As per the points of interest, it doesn't have to create negative pulses for negative cycle. In this way, no unnecessary conditions are put to control the negative cycle voltage. Instead, the reversing full bridge inverter does this work, and the required level is created by the high switching recurrence segment of the inverter. At that point [9], this level is changed over to negative polarity as indicated by the output voltage prerequisites. This topology is repetitive and adaptable in the exchanging succession. Distinctive exchanging modes in creating the required levels for an eleven-level RV topology inverter are indicated in tabular format in Table 1.

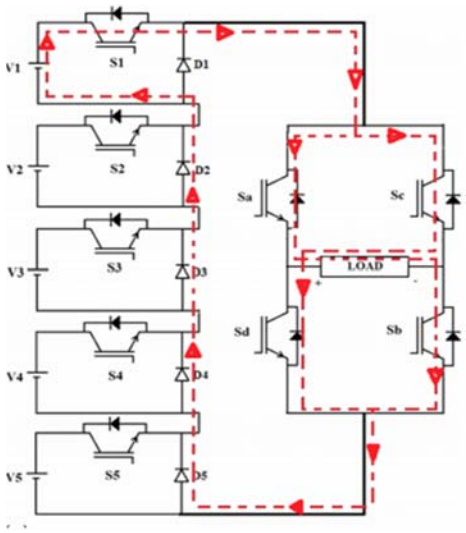

Figure 4. Working of R-V topology inverter

Table. 1 Switching table for proposed system

Levels	voltage	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	5Vdc	1	1	1	1	1	1	0	0	1
2	4Vdc	0	1	1	1	1	1	0	0	1
3	3Vdc	0	0	1	1	1	1	0	0	1
4	2Vdc	0	0	0	1	1	1	0	0	1
5	Vdc	0	0	0	0	1	1	0	0	1
6	0	0	0	0	0	0	0	0	0	0
7	-Vdc	0	0	0	0	1	0	1	1	0
8	-2Vdc	0	0	0	1	1	0	1	1	0
9	-3Vdc	0	0	1	1	1	0	1	1	0
10	-4Vdc	0	1	1	1	1	0	1	1	0
11	-5Vdc	1	1	1	1	1	0	1	1	0

The switching sequence can be explained likewise. When S1 is on, the diode D1 is in a reverse bias condition and current flows through S1 and generates the level at Vdc. When S2 is on and it generates the level at 2Vdc D2 is reverse biased. The same operation continues for other switches also, when the main switch is on and the diode get reverse biased. S3 is generates the level at 3Vdc at on condition. When S4 generates the level at 4Vdc during it operation. When S5 is on and the current flows through S5 and generates the level at 5Vdc, the diode D5 are in a reverse bias condition. Likewise, positive levels are generated. This positive output is fed to the reversing inverter that reverses the positive part to generate negative levels.

4. SIMULATION MODEL FOR REVERSE VOLTAGE TOPOLOGY MULTILEVEL INVERTER

The MATLAB simulation has been shown for RV topology 11-Level Multilevel inverter is shown in the Figure 5. This design has been simulated by reverse voltage topology. The output for the designed topology for proposed model is shown in Figure 6. The simulation output for 11-Level Multilevel Inverter has been shown. Each level has been obtained from Vdc to 5Vdc and vice versa.

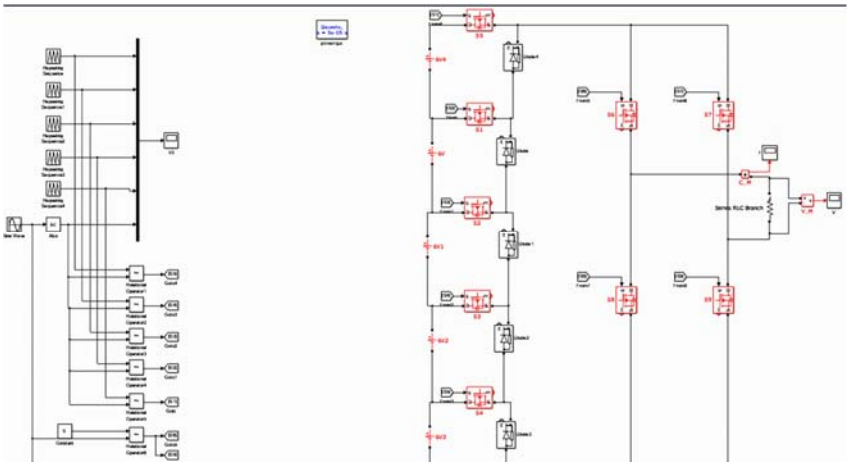

Figure 5. MATLAB simulation diagram for RV topology multilevel inverter

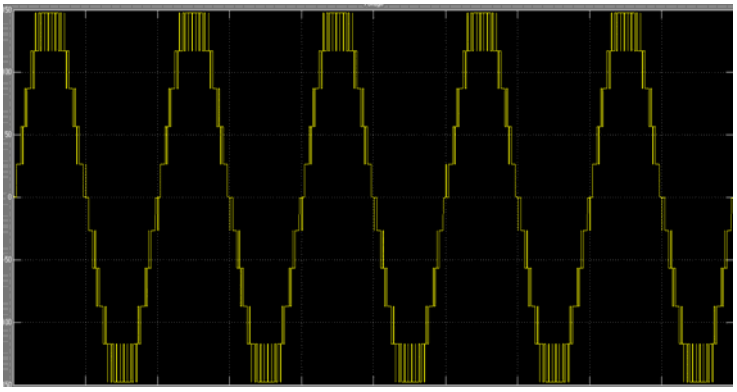

Figure 6. The simulation output for 11 level MLI

5. PWM TECHNIQUE

PWM Technique is called Pulse Width Modulation. Pulse width modulation (PWM) is a regulation procedure or method utilized as a part of most frameworks for encoding the amplitude of a specific signal to a pulse width. In spite of the fact that it is mainly used for communications, the fundamental motivation behind this procedure is to control the power that is provided to different kinds of electric drives. PWM is utilized for controlling the more number of computerized motions keeping in mind the end goal to control gadgets and application that requires current or voltage [16, 17]. It basically controls the measure of intensity, in the viewpoint of voltage components [8]. That is given to a specific gadget by turning the on-off periods of a specific digital signal rapidly and thus differing the width of the on stage or duty cycle [18].

Out of many pulse width modulation techniques, SPWM Technique has been utilized. SPWM is a technique for pulse width balance utilizes as a part of inverters. The inverter delivers an alternating output voltage from a Direct input by using switching circuits to mimic a sinusoidal wave frame, by creating at least one square pulse of voltage per half cycle. In the event that the width of the pulses is balanced as methods for managing the output voltage, henceforth it is said that the pulse width is modulated. With sine or sine like pulses are delivered per half cycle. The pulse close to the edges at the half cycle are smaller and close to the focal point of the half cycle accordingly there is an adjustment in adequacy [19, 20]. To adjust the successful output voltage, the width of all pulse are expanded or diminished while keeping up the sinusoidal proportionality as it seems to be. In this paper the SPWM Technique has been utilized. In traditional multilevel inverters for 11 voltage levels 10 carrier signals are required but yet for this present system only 5 carrier signals are needed to generate 11 levels. Here one sinusoidal carrier and five triangular wave carrier has been used and shown in Figure 7. For modulation index near unity resultant output the THD for output voltage is 11.46% and it is shown in Figure 8.

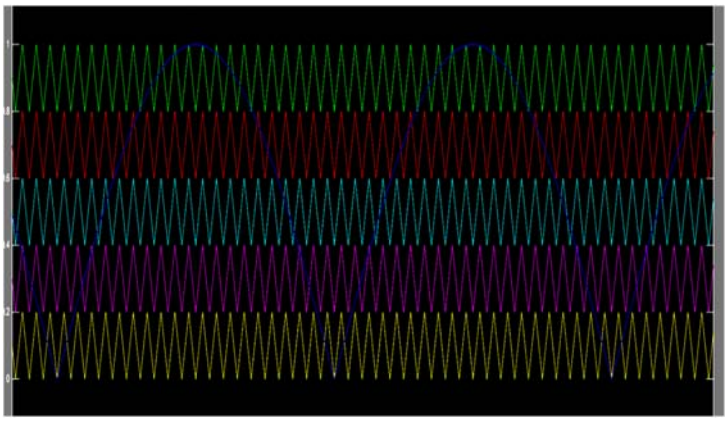

Figure 7. Carrier signal

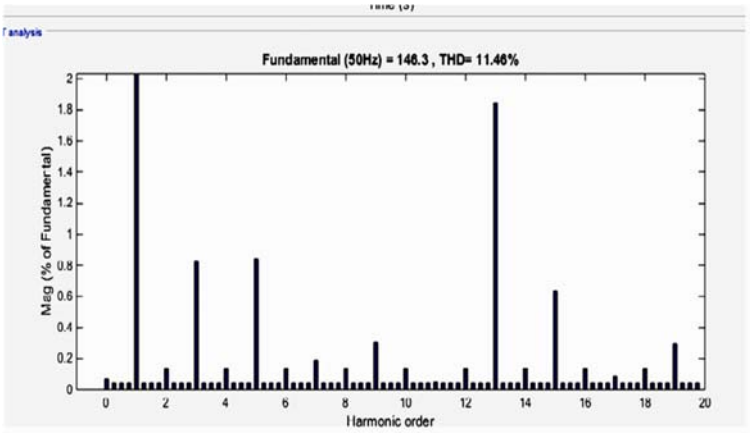

Figure 8 THD analysis

6. EXPERIMENTAL APPROACH OF THE PROPOSED MODEL

The hardware setup of proposed model has shown in Figure 9. Solar cell gives an output voltage of 19.17V that is fed to a Buck Converter which steps down the voltage. The Buck converter has been controlled by MPPT Algorithm that is embedded on DSPIC30F2010 controller. The output part of the Buck Converter is connected to a 12V battery. The reason behind using the 12V battery is that MPPT doesn't give constant power. As the total power output of a solar cell depends on irradiation so MPPT tracks the maximum power at different irradiations. Hence to obtain maximum power the battery has been used. On the next half, the output of DSPIC30F2010 is 5V. But in order to trigger the MOSFET gate 15V is needed as a result TLP 250 driver circuit is used. TLP 250 enhances the current and in turns it gives path to voltage. As, the MOSFETs are triggered, it starts to generate the levels.

Figure 9. Experimental Setup of Proposed Topology

7. CONCLUSION

In this paper, a newly proposed inverter topology has been proposed. In comparing with the conventional topology, the proposed topology has superior in characteristics and performance. This has less number of number of switches and isolated dc sources, voltage stability, manageable requirements and dependability. Simulated results also illustrate the overall performance and effectiveness of the proposed topology. The experimental results also explaining the performance of the proposed reverse voltage topology MLI. The SPWM controller also has less complexity since it uses just five carriers for PWM control. Both the simulated and experimental results are matching together. As sustainable power sources can be utilized for multilevel inverter, photovoltaic cell has been utilized.

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